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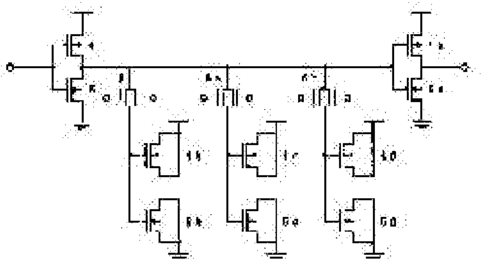
(54) DELAY CIRCUIT AND DIGITAL PHASE LOCK CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To realize different delay times for the delay circuit by adopting a variable capacitor for a capacitor connected between a 1st inverting buffer and a 2nd inverting buffer.

SOLUTION: A 1st inverting buffer is made up of a 1st P-channel field effect transistor 4 and a 1st N-channel field effect transistor 5 and a 2nd inverting buffer is made up of a 2nd P-channel field effect transistor 4a and a 2nd N- channel field effect transistor 5a. Furthermore, capacitors being P-channel field effect transistors 4b-4d are connected in parallel with capacitors being N-channel field effect transistors 5b-5d respectively. Then 1st-3rd transmission gates 6, 6a, 6b act like switches. Thus, the delay circuit is realized, in which its delay time is made variable by the selection of a transmission gate to be switched on.



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CLAIMS

[Claim(s)]
[Claim 1]A delay circuit comprising:
The first buffer gate.
The second buffer gate.
Composition which has at least one series connection body of a switch and a capacitor which are connected between points set as a signal wire which connects an output terminal of the first buffer gate, and an input terminal of the second buffer gate, and predetermined potential.

[Claim 2]A delay circuit comprising:
A parallel connection body which connected a series connection body of a buffer gate and a switch in parallel.
A capacitor connected between points set as an output terminal of this parallel connection body, and predetermined potential.
A buffer gate where an input terminal is connected to a different output terminal of this parallel connection body from a buffer gate which constitutes this series connection body.

[Claim 3]A delay circuit comprising:
The first buffer gate.
The second buffer gate.
A capacitor connected between points set as a signal wire which connects an output terminal of this first buffer gate, and an input terminal of this second buffer gate, and predetermined potential.
The third buffer gate where an input terminal is connected to an input terminal of this first buffer gate, and an output terminal is connected to an input terminal of this second buffer gate, The first switch inserted in a terminal by the side of a current inflow of this third buffer gate in series, A full swing circuit which has the composition which has the second switch inserted in the current drain side of this third buffer gate in series, and controls opening and closing of this first and the second switch by output potential of this second buffer gate, and controls conversely opening and closing of this first and the second switch.

[Claim 4]In the delay circuit according to claim 1, the full swing circuit according to claim 3 is provided, A delay circuit connecting to an input terminal of said first buffer gate an input terminal of the third buffer gate that constitutes this full swing circuit, and connecting to an input terminal of said second buffer gate an output terminal of the third buffer gate that constitutes this full swing circuit.
[Claim 5]Inside of a buffer gate which constitutes a series connection body connected to said parallel in the delay circuit according to claim 2, A buffer gate except a buffer gate of at least 1 is replaced by the full swing circuit according to claim 3, An input terminal of said third buffer gate that constitutes this full swing circuit is connected to an input terminal of said parallel connection body, An output terminal of said third buffer gate that constitutes this full swing circuit is connected to an output terminal of said parallel connection body, Opening and closing of the second switch are controlled by output potential of said different buffer gate from a buffer gate which constitutes said series connection body for a start [said] which constitutes this full swing circuit, And a delay circuit controlling conversely a switching condition of this first and the second switch, and inserting a switch in the current inflow [of this full swing circuit], and current drain side in series further.
[Claim 6]Inside of a buffer gate which constitutes a series connection body connected to said parallel in the delay circuit according to claim 2, A buffer gate except a buffer gate of at least 1 is replaced by the full swing circuit according to claim 3, An input terminal of said third buffer gate that constitutes this full swing

circuit is connected to an input terminal of said parallel connection body, An output terminal of said third buffer gate that constitutes this full swing circuit is connected to an output terminal of said parallel connection body, Opening and closing of the second switch are controlled by output potential of said different buffer gate from a buffer gate which constitutes said series connection body for a start [said] which constitutes this full swing circuit, And a delay circuit connecting a transistor which achieves a switch function which controls conversely a switching condition of this first and the second switch, and by which opening and closing are further controlled conversely in parallel with a transistor of 2 which achieves a switch function in this full swing circuit.

[Claim 7]Are the delay circuit according to any one of claims 1 to 6, and said capacitor, A P-CH type field effect transistor from which a drain and sauce of at least 1 are connected, and it was made for a connected drain and sauce to certainly become high potential from a gate electrode, A delay circuit being the capacitor to which a drain and sauce of this P-CH type field effect transistor and the same number were connected to, and a connected drain and sauce connected in parallel a N-CH type field effect transistor it was made to certainly become low voltage from a gate electrode.

[Claim 8]The delay circuit according to any one of claims 1 to 7 is applied to a ring oscillator, Calculation of an up-and-down counting circuit is controlled by an output of a phase comparison circuit mentioned later, In [choose a time delay of this delay circuit by a count output of this up-and-down counting circuit, choose oscillating frequency of this ring oscillator, carry out dividing of the oscillation output of this ring oscillator in a frequency divider containing the division ratio 1, and] a phase comparator, A digital phase locking circuit comparing a phase of these dividing outputs and an input clock.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a delay circuit and a digital phase locking circuit, especially, can realize arbitrary time delays and relates to a delay circuit with little duty ratio degradation of a data signal, and a digital phase locking circuit with few phase errors using it.
[0002]In a digital circuit, it is necessary to adjust the phase of a clock and a data signal, and the phase between data in many cases. Although such phase adjustment is performed by using a delay circuit or hitting a data signal again with a clock etc., this invention relates to the former. And it is requested for a delay circuit that arbitrary time delays are realizable, the waveform deterioration during input and output of a delay circuit, and that there is especially little duty ratio degradation.
[0003]In a digital phase locking circuit, the frequency of the oscillator which a digital phase locking circuit builds in is controlled by phase relation of the signal and input clock which carried out dividing of the output frequency of the oscillator, and the clock in sync with an input clock is outputted. Therefore, the phase error of a digital phase locking circuit is determined by the adjustment accuracy of the frequency of the oscillator which a digital phase locking circuit builds in. For the purpose, it is required for the adjustment accuracy of the time delay of the delay circuit applied to that oscillator to be high, i.e., arbitrary time delays are realizable in that delay circuit.
[0004]
[Description of the Prior Art]Drawing 12 is the conventional delay circuit (the 1). As for 1, as for the first inverting buffer and 1a, in drawing 12, the second inverting buffer and 3 are capacitors.
[0005]In the composition of drawing 12, operation is explained as that by which a square wave is impressed to an input terminal. Since the first inverting buffer makes a capacitor discharge when a square wave is a level of "1", the terminal voltage of a capacitor falls. If the terminal voltage of this capacitor reaches the threshold of the second inverting buffer, the second inverting buffer will turn off and an output level will be set to "1." On the other hand, since the first inverting buffer charges a capacitor when a square wave is a level of "0", the terminal voltage of a capacitor rises. If the terminal voltage of this capacitor reaches the threshold of the second inverting buffer, and an output level will be set to "0". [the second inverting buffer] Therefore, if the answering delay time of an inverting buffer can be disregarded, time until the terminal voltage of a capacitor reaches the threshold of the second inverting buffer from the standup of an input signal will turn into a time delay of the composition of drawing 12. Actually, since the answering delay time of the second inverting buffer cannot be disregarded, either, The time delay of the composition of drawing 12 turns into a time delay of the composition of the time which added the answering delay time of the second inverting buffer to time until the terminal voltage of a capacitor reaches the threshold of the second inverting buffer from the standup of an input signal of drawing 12. And when the composition of drawing 12 is constituted in large scale integration circuit, the time delay is immobilization.
[0006]Drawing 13 is the conventional delay circuit (the 2). As for 1, as for the first inverting buffer and 1a, in drawing 13, the second inverting buffer and 3 are capacitors.
[0007]As for the composition of drawing 13, the first inverting buffer and the second inverting buffer are constituted in large scale integration circuit, and the capacitor shows the case where it is provided out of the large scale integration circuit. Although it is for shortening wiring from a capacitor to a ground and acquiring an exact time delay, that the ground to which one terminal of a capacitor is connected in drawing 13 is for the ground in large scale integration circuit may ground out of large scale integration circuit, as long as it cares about a wire length. Rather, there is an advantage which can lessen the pin count of large scale integration circuit required in order that this gentleman may form a capacitor. The feature of the composition of drawing 13 is at the point as for which a time delay is made variable, if the capacity of a

capacitor is adjusted for writing a capacitor to external.
[0008]Drawing 14 is the conventional delay circuit (the 3). In drawing 14, the first inverting buffer and 1a 1 The second inverting buffer, The third inverting buffer and 1c 1b The fourth inverting buffer, The fifth inverting buffer and 1e 1 d The sixth inverting buffer, The seventh inverting buffer and 1 g 1 f The eighth inverting buffer, The ninth inverting buffer and 1i 1 h The tenth inverting buffer, 2 -- the first switch and 2a -- the second switch and 2b -- the third switch and 2c -- the fifth switch and 2e are [the ninth switch and 2i of the seventh switch and 2 g (the fourth switch and 2 d) (the sixth switch and 2 f) (the eighth switch and 2 h)] the tenth switch.
[0009]In the composition of drawing 14, a switch, the second switch, the first switch and fourth switch, [third] The fifth switch, the sixth switch and the seventh switch, the eighth switch and the ninth switch, and tenth switch are a switch which interlocks and moves conversely mutually, and the composition of drawing 14 serves as a delay circuit variable in a time delay by the opening and closing control of these switches. For example, if the first switch is carried out to one and the second switch is turned OFF, an input signal will reach an output terminal only via the first inverting buffer and the second inverting buffer. If the second switch is carried out to one and the third switch is carried out to one, an input signal will reach an output terminal through the first inverting buffer, the second inverting buffer, the third inverting buffer, and the fourth inverting buffer. That is, the composition of drawing 14 is a delay circuit which makes the time delay of the second inverting buffer a unit, and can adjust a time delay.
[0010]
[Problem(s) to be Solved by the Invention]The time delay from which the composition of drawing 12 constructs in large scale integration circuit, and is obtained by the composition of drawing 12 at a ********** case is immobilization. Therefore, when used as a delay circuit, adjustment of a time delay is impossible, and frequency is fixed when the composition of drawing 12 is used for a digital phase locking circuit.
[0011]In the composition of drawing 13, when used as a delay circuit, it becomes possible to adjust a time delay by adjusting the capacity of an external capacitor, and when the composition of drawing 13 is used for a digital phase locking circuit, the advantage as for which frequency is made variable arises. However, since many terminals of large scale integration circuit are needed when the part which adjusts the time delay of a delay circuit, and the part which adjusts the frequency of a digital phase locking circuit increase, there is a possibility of driving large scale integration circuit into the state of a terminal neck.
[0012]The composition of drawing 14 needs many inverting buffers to the advantage which can adjust a time delay, Since it must pay needing many terminals of large scale integration circuit for delay adjustment as compensation and also the minimum step of the amount of delay adjustments becomes two steps of yne baaing buffers, it does not turn against fine adjustment of delay.
[0013]Drawing 15 is a figure explaining the problem of the conventional delay circuit, and explains the problem especially in the composition of drawing 12 and drawing 13. In drawing 15, the terminal voltage of a capacitor and (3) are output signals the input signal whose duty ratio is 50% (1), and (2).
[0014]The current to which the first inverting buffer charges a capacitor, and the current of a problem made to discharge are not enough, It happens that terminal voltage of a capacitor cannot reach V_{SS} which is ground voltage while an input signal is "1", When it happens that terminal voltage of a capacitor cannot reach V_{DD} which is power supply voltage while an input signal is "0", the duty ratio of an output signal is not [hear / I / that it becomes] 50%, and there is. That is, while an input signal is "1", it is made to discharge a capacitor and the terminal voltage of a capacitor falls, but before reaching V_{SS}, input voltage will change to "0." Since a capacitor will be charged if input voltage is set to "0", the terminal voltage of a capacitor rises, but before reaching V_{DD} too, input voltage will change to "1." And since the characteristics of the transistor which sends the current which makes a capacitor discharge, and the transistor which sends the current which charges a capacitor differ, it is common that the inclinations of discharge and charge differ. for this reason -- case the inclination of the charge shown in drawing 15 is smaller -- the average value of the terminal voltage of a capacitor -- steps -- it becomes low. Under the influence of these both sides, all the time of ** of an output signal, **, and ** will differ, and a duty ratio will shift from 50%. Although the thin solid line shows the case where the terminal voltage of a capacitor can go between V_{DD} and V_{SS} back and forth with a grinding sound between "1" of an input signal, and "0", it turns out that an output wave is considerably different. In the case of drawing 15, a waveform becomes fixed after **.
[0015]That this problem should be solved, this invention can realize arbitrary time delays and an object of this invention is to provide a delay circuit with little duty ratio degradation of a data signal, and a digital

phase locking circuit with few phase errors using it.

[0016]

[Means for Solving the Problem]Drawing 1 is the first principle of a delay circuit of this invention. in drawing 1 -- 1 -- the first inverting buffer and 1a -- as for the third switch and 3, the first switch and 2a are [the second switch and 2b / the second capacitor and 3b of the first capacitor and 3a] the third capacitor the second inverting buffer and 2.

[0017]Although composition of drawing 1 carries out the same operation as composition of drawing 12 fundamentally, Two or more capacitors are prepared, capacity of a capacitor connected by opening and closing of a switch connected to this capacitor and series between the first inverting buffer and the second inverting buffer is made variable, and the feature is that it made it composition which can realize a different time delay. In the case of drawing 1, if it is made for all capacity of a capacitor of 3 to differ, it is possible to realize eight kinds of time delays also including a case where a capacitor is not connected. That is, in composition of drawing 1, there are no restrictions in opening and closing of a switch.

[0018]Drawing 2 is the second principle of a delay circuit of this invention. In drawing 2, the first inverting buffer and 1a 1 The second inverting buffer, 1b -- the third inverting buffer and 1c -- as for the fourth switch and 3, as for the second switch and 2b, the fifth inverting buffer and 2 are [the first switch and 2a / the third switch and 2c] capacitors. [of the fourth inverting buffer and 1 d] It must be made for either the first thru/or the fourth switch to be turned on.

[0019]Except for the first inverting buffer and the second inverting buffer, the feature of composition of drawing 2 by opening and closing of a switch connected to an inverting buffer of the third henceforth in series. It is in a point of adjusting a time delay, by adjusting the number of inverting buffers which charge a capacitor or are made to discharge. That is, since current which charges a capacitor or is made to discharge will become large if there are many inverting buffers connected, it is possible by adjusting the number of inverting buffers to adjust a time delay. And if all the characteristics of the third, fourth, and fifth inverting buffer differ for a start, it is possible to realize 15 kinds of time delays. By increasing the number of inverting buffers and gathering speed of charge of a capacitor, and discharge, An input signal can descend [terminal voltage of a capacitor] now even to V_{ss} from V_{DD} between "1", Since an input signal can go up [terminal voltage of a capacitor] now even from V_{SS} to V_{DD} between "1", an initial condition of charge of a capacitor and discharge becomes the same always. Therefore, even though it was influenced by inclinations of charge of a capacitor and discharge differing, a duty ratio of an output signal becomes fixed, If it is a range which can disregard a difference of an inclination of charge of a capacitor, and discharge, it will become possible for a duty ratio of an output signal to be about 50%, and to acquire a waveform of a stable output signal.

[0020]Drawing 3 is the third principle of a delay circuit of this invention. In drawing 3, the first inverting buffer and 1a 1 The second inverting buffer, 3 is [the first N-CH type field effect transistor and 5a of the first P-CH type field effect transistor and 4a] the second N-CH type field effect transistor the second P-CH type field effect transistor and 5 a capacitor and 4. A circuit constituted by this first P-CH type field effect transistor 4, the second P-CH type field effect transistor 4a, the first N-CH type field effect transistor 5, and the second N-CH type field effect transistor 5a will be called a full swing circuit.

[0021]The first P-CH type field effect transistor 4 and the first N-CH type field effect transistor 5 constitute an inverting buffer, charge a capacitor or are made to discharge it in composition of drawing 3. The second P-CH type field effect transistor 4a and the second N-CH type field effect transistor 5a operate as a switch, and one [the field effect transistor / current] and turn off current of an inverting buffer.

[0022]Although it has composition which uses the field effect transistors 4a and 5a in drawing 3, and one [composition / current] and turns off current of the first P-CH type field effect transistor 4 and the first N-CH type field effect transistor 5, A transmission gate etc. can also be used instead of the field effect transistors 4a and 5a.

[0023]Drawing 4 is a figure explaining operation of composition of drawing 3, and, as for (1), terminal voltage of a capacitor and (3) are output signals an input signal of 50% of a duty ratio, and (2). First, when an input signal is [an output signal] "0" in "1", the first P-CH type field effect transistor 4 and the second N-CH type field effect transistor 5a are come by off. Although the first N-CH type field effect transistor 5 and the second P-CH type field effect transistor 4a are the conditions which can be turned on at this time, Since the first P-CH type field effect transistor 4 and the second N-CH type field effect transistor 5a are come by off, a full swing circuit does not carry out also charging a capacitor and also making a capacitor discharge. Therefore, the first inverting buffer is making a capacitor discharge during this period. If terminal voltage of a capacitor reaches a threshold of the second inverting buffer by this discharge, an output of the second inverting buffer will be set to "1", and an input signal and an output signal will be set to "1." The first P-CH type field effect transistor 4 and the second P-CH type field effect transistor 4a are come in this period by off, Since the first N-CH type field effect transistor 5 and the second N-CH type field effect transistor 5a are turned on, a full swing circuit accelerates discharge of a capacitor. Therefore, terminal voltage of a capacitor falls quickly and reaches V_{SS}. And when an input signal falls in "0", since an output signal is still "1", the first P-CH type field effect transistor 4 and the second N-CH type field effect transistor 5a are the conditions which can be turned on, but. Since the first N-CH type field effect transistor 5 and the second P-CH type field effect transistor 4a are off, a full swing circuit does not carry out also charging a capacitor or also making it discharge. Therefore, the first inverting buffer has charged a capacitor in this period. If terminal voltage of a capacitor reaches a threshold of the second inverting buffer by this charge, an output signal of the second inverting buffer will be set to "0", and an input signal and an output signal will be set to "0." The first P-CH type field effect transistor 4 and the second P-CH type field effect transistor 4a are come on by this period, and the first N-CH type field effect transistor 5 and the second N-CH type field effect transistor 5a are come by off. Therefore, a full swing circuit circuit accelerates charge of a capacitor, and terminal voltage of a capacitor rises quickly and reaches V_{DD}. And the above-mentioned operation is repeated with a repetition of an input signal. Therefore, as for conditions at the time of discharge starting of a capacitor, conditions at the time of charge starting of a capacitor also always become fixed always uniformly. For this reason, if an output signal has a difference in charging current and discharge current of an inverting buffer, although a duty ratio will shift from 50%, a waveform always becomes fixed every cycle and a gap of a duty ratio becomes smaller than the conventional delay circuit. If it is a range which can disregard a difference of charging current of an inverting buffer, and discharge current, a duty ratio of an output signal will be about 50%. When charge and discharge are late and terminal voltage of a capacitor cannot reach at least one side of V_{DD} and V_{SS} in the conventional delay circuit, Even if it is a range which can disregard a difference of charging current of an inverting buffer, and discharge current, it turns out that a duty ratio of an output signal has a large duty ratio improvement effect as compared with not becoming 50%.

[0024]

[Embodiment of the Invention]Drawing 5 is a first embodiment of the delay circuit of this invention. In drawing 5, the first P-CH type field effect transistor and 4a 4 The second P-CH type field effect transistor, The third P-CH type field effect transistor and 4c 4b The fourth P-CH type field effect transistor, The fifth P-CH type field effect transistor and 5 4 d The first N-CH type field effect transistor, The second N-CH type field effect transistor and 5b 5a The third N-CH type field effect transistor, As for the fifth N-CH type field effect transistor and 6, 5c is [the second transmission gate and 6b of the first transmission gate and 6a (the fourth N-CH type field effect transistor and 5 d)] the third transmission gate.

[0025]In the composition of drawing 5, the first P-CH type field effect transistor 4 and the first N-CH type field effect transistor 5 constitute the first inverting buffer of drawing 1, The second P-CH type field effect transistor 4a and the second N-CH type field effect transistor 5a constitute the second inverting buffer of drawing 1. The third P-CH type field effect transistor 4b, the fourth P-CH type field effect transistor 4c, 4 d of fifth P-CH type field effect transistor, the third N-CH type field effect transistor 5b, The fourth N-CH type field effect transistor 5c and 5 d of fifth N-CH type field effect transistor, Although the drain and sauce which the drain and sauce which sauce was connected with the drain, respectively and were connected in the case of the P-CH type field effect transistor were connected to the power supply (high potential side), and were connected in the case of the N-CH type field effect transistor are connected to the ground (low voltage side), These constitute the gate, and the connected drain and the capacitor using the capacity between sauce. The drain and sauce which were connected in the case of the P-CH type field effect transistor are connected to a power supply (high potential side) here, In the case of a N-CH type field effect transistor, connecting the connected drain and sauce to a ground (low voltage side), Since it is with potential relation with each gate electrode, and the gate electrode is connected in this case at the node of the inverting buffer of 2, and it is for securing the capacity of a capacitor as an electric charge effective in a channel section stagnates, it is indispensable connection. Since what is necessary is just deciding the potential between a gate electrode or the connected drain, and sauce that an electric charge effective in the channel of each transistor stagnates, speaking still more generally, What is necessary is for what is necessary to be just to make it the drain and sauce which were connected certainly become high potential from a gate electrode, and just to make it the drain and sauce which were connected certainly become low voltage from a gate electrode by a N-CH type field effect transistor by a P-CH type field effect transistor. Carrying out multiple connection of the capacitor by a P-CH type field effect transistor and the capacitor by a N-CH type field effect transistor, The capacity variation by the voltage between a gate, and the connected drain and sauce large one in a P-CH type field effect transistor or a N-CH type field effect transistor simple substance, It is for oppressing a capacity variation using carrying out a reverse capacity variation by the P-CH type field effect transistor and a N-CH type field effect transistor. And the first thru/or the third transmission gate achieve the function of the switch of drawing 1. Therefore, the composition of drawing 5 serves as a delay circuit which changes a time delay by selection of the transmission gate made one.

[0026]If the third thru/or fifth P-CH type field effect transistor is made into the same size and the third thru/or fifth N-CH type field effect transistor is realized in the same size, The time delay except the time delay of the inverting buffer can be chosen from among 0tau, 2tau, and 3tau if the time delay at the time of making the transmission gate of 1 one is set to tau. The size of the fourth P-CH type field effect transistor is doubled to the size of the third P-CH type field effect transistor, Increase the size of the fifth P-CH type field effect transistor 4 times, and similarly, If the size of the fourth N-CH type field effect transistor is doubled to the size of the third N-CH type field effect transistor and the size of the fifth N-CH type field effect transistor is increased 4 times, If a time delay when only the first transmission gate is made one is set to tau, the time delay except the time delay of the inverting buffer, It can choose from among 0tau, 2tau, 3tau, 4tau, 5tau, 6tau, and 7tau by whether which transmission gate is made one. Thus, the number of the time delays it is more nearly selectable not to make the same the size of the third thru/or fifth P-CH type field effect transistor and a N-CH type field effect transistor can be increased. The size of the fourth P-CH type field effect transistor and a N-CH type field effect transistor is made into 1/10 to the size of the third P-CH type field effect transistor and the third N-CH type field effect transistor, If the size of the fifth P-CH type field effect transistor and a N-CH type field effect transistor is set to one fifth, The time delay except the time delay of the inverting buffer can be chosen from among tau+0.1tau, tau+0.2tau, and tau+0.3tau near tau, and can tune a time delay finely.

[0027]Drawing 6 is a second embodiment of the delay circuit of this invention. In drawing 6, the first P-CH type field effect transistor and 4a 4 The second P-CH type field effect transistor, The third P-CH type field effect transistor and 4c 4b The fourth P-CH type field effect transistor, The fifth P-CH type field effect transistor and 4e 4 d The sixth P-CH type field effect transistor, The first N-CH type field effect transistor and 5a 5 The second N-CH type field effect transistor, The third N-CH type field effect transistor and 5c 5b The fourth N-CH type field effect transistor, The fifth N-CH type field effect transistor 5e 5 d The sixth N-CH type field effect transistor, As for the first transmission gate and 6a, the third transmission gate and 6c of the second transmission gate and 6b are the fourth transmission gate 6.

[0028]In the composition of drawing 6, the first P-CH type field effect transistor 4, the first N-CH type field effect transistor 5 and the third P-CH type field effect transistor 4b, and the third N-CH type field effect transistor 5b, The fourth P-CH type field effect transistor 4c and the fourth N-CH type field effect transistor 5c, The combination of 4 d of fifth P-CH type field effect transistor, and 5 d of fifth N-CH type field effect transistor, It corresponds to the third, fourth, and fifth inverting buffer for a start in drawing 2, respectively, The combination of the second P-CH type field effect transistor 4a and the second N-CH type field effect transistor 5a corresponds to the second inverting buffer of drawing 2, 4 d of sixth P-CH type field effect transistor and 5 d of sixth N-CH type field effect transistor correspond to a capacitor, and the first thru/or the fourth transmission gate 6 thru/or 6c correspond to the first of drawing 2 thru/or the fourth switch. Some first thru/or fourth transmission gate must make one one.

[0029]And the composition of drawing 6 becomes a delay circuit with a variable time delay with the combination of whether to make which transmission gate one. For example, the first P-CH type field effect transistor and the first N-CH type field effect transistor are received, The size of the third P-CH type field effect transistor and the third N-CH type field effect transistor is made into twice, If the size of the fourth P-CH type field effect transistor and a fourth N-CH type field effect transistor is made into 4 times and the size of the fifth P-CH type field effect transistor and the fifth N-CH type field effect transistor is made into 8 times, Since the current driving force of each inverting buffer is proportional to the size of a field effect transistor, the time delay except the time delay of the second inverting buffer of the composition of a figure can be tau (1/n) (here, n is integer of 1 to 15) 15-copy Rika chosen.

[0030]Drawing 7 is a third embodiment of the delay circuit of this invention. In drawing 7, the first P-CH type field effect transistor and 4a 4 The second P-CH type field effect transistor, The third P-CH type field effect transistor and 4c 4b The fourth P-CH type field effect transistor, The fifth P-CH type field effect transistor and 4e 4 d The sixth P-CH type field effect transistor, The seventh P-CH type field effect transistor and 4 g 4 f The eighth P-CH type field effect transistor, The ninth P-CH type field effect transistor and 4i 4 h The tenth P-CH type field effect transistor, The first N-CH type field effect transistor and 5a 5 The second N-CH type field effect transistor, The third N-CH type field effect transistor and 5c 5b The fourth N-CH type field effect transistor, The fifth N-CH type field effect transistor and 5e 5 d The sixth N-CH type field effect transistor, The seventh N-CH type field effect transistor and 5 g 5 f The eighth N-CH type field effect transistor, As for the first NOT gate and 7a, the ninth N-CH type field effect transistor and 5i are [the third NOT gate and 7c of 5 h of the second NOT gate and 7b] the fourth NOT gate the tenth N-CH type field effect transistor and 7.

[0031]In the composition of drawing 7, the group of the first P-CH type field effect transistor 4 and the first N-CH type field effect transistor 5 corresponds to the first inverting buffer of drawing 2, The group of the second P-CH type field effect transistor 4a and the second N-CH type field effect transistor 5a corresponds to the second inverting buffer of drawing 2, The group of the third P-CH type field effect transistor 4b and the third N-CH type field effect transistor 5b, The group of the fourth P-CH type field effect transistor 4c and the fourth N-CH type field effect transistor 5c, The group of 4 d of fifth P-CH type field effect transistor and 5 d of fifth N-CH type field effect transistor corresponds to the third of drawing 2 thru/or the fifth inverting buffer, The group of the sixth P-CH type field effect transistor 4e and the sixth N-CH type field effect transistor 5e, The group of 4 f of seventh P-CH type field effect transistor, and 5 f of seventh N-CH type field effect transistor, The group of the group of 4 g of eighth P-CH type field effect transistor and 5 g of eighth N-CH type field effect transistor, 4 h of ninth P-CH type field effect transistor, and 5 h of ninth N-CH type field effect transistor, Corresponding to the first of drawing 2 thru/or the fourth switch, respectively, the group of the tenth P-CH type field effect transistor 4i and the tenth N-CH type field effect transistor 5i corresponds to the capacitor of drawing 3. Also in drawing 7, one of switches must be one. And it is only that the composition of a switch differs and the composition of drawing 7 is intrinsically equivalent to the composition of drawing 6. That is, and it turns off. [the current of the field effect transistors / in / drawing 7 / 4 and 5 from which the sixth P-CH type field effect transistor 4e and the sixth N-CH type field effect transistor 5e constitute an inverting buffer] [direct] On the other hand, the switch by the transmission gate of drawing 6 is a gestalt which one [a gestalt / output potential] and turns off the output potential of an inverting buffer. However, there is no change in controlling the signal which appears by operation of a switch also in any output side of an inverting buffer or case.

[0032]Drawing 8 is a fourth embodiment of the delay circuit of this invention. In drawing 8, the first P-CH type field effect transistor and 4a 4 The second P-CH type field effect transistor, The third P-CH type field effect transistor and 4c 4b The fourth P-CH type field effect transistor, The fifth P-CH type field effect transistor and 4e 4 d The sixth P-CH type field effect transistor, The seventh P-CH type field effect transistor and 4 g 4 f The eighth P-CH type field effect transistor, The first N-CH type field effect transistor and 5a 5 The second N-CH type field effect transistor, The third N-CH type field effect transistor and 5c 5b The fourth N-CH type field effect transistor, The fifth N-CH type field effect transistor and 5e 5 d The sixth N-CH type field effect transistor, The seventh N-CH type field effect transistor and 5 g 5 f The eighth N-CH type field effect transistor, The first transmission gate and 6a 6 The second transmission gate, As for the fourth transmission gate and 6 d, 6b is [the third transmission gate and 6c / the sixth transmission gate and 6 f of the fifth transmission gate and 6e] the seventh transmission gate.

[0033]Since this will combine the composition of drawing 5, and the composition of drawing 6 so that clearly if drawing 8 is seen, detailed explanation is omitted, but in the composition of drawing 8, one of transmission gates must be one.

[0034]Drawing 9 is a fifth embodiment of the delay circuit of this invention. In drawing 9, the first P-CH type field effect transistor and 4a 4 The second P-CH type field effect transistor, The third P-CH type field effect transistor and 4c 4b The fourth P-CH type field effect transistor, The fifth P-CH type field effect transistor and 4e 4 d The sixth P-CH type field effect transistor, The seventh P-CH type field effect transistor and 4 g 4 f The eighth P-CH type field effect transistor, The ninth P-CH type field effect transistor and 4i 4 h The tenth P-CH type field effect transistor, The eleventh P-CH type field effect transistor and 4k 4j The twelfth P-CH type field effect transistor, The first N-CH type field effect transistor and 5a 5 The second N-CH type field effect transistor, The third N-CH type field effect transistor and 5c 5b The fourth N-CH type field effect transistor, The fifth N-CH type field effect transistor and 5e 5 d The sixth N-CH type field effect transistor, The ninth N-CH type field effect transistor and 5i the seventh N-CH type field effect transistor and 5 g the eighth N-CH type field effect transistor and 5 h 5 f The tenth N-CH type field effect transistor, As for the twelfth N-CH type field effect transistor and 7, 5j is [the eleventh N-CH type field effect transistor and 5k / the second NOT gate and

7b of the first NOT gate and 7a] the third NOT gate.

[0035]In the composition of drawing 9, the group of the first P-CH type field effect transistor 4 and the first N-CH type field effect transistor 5 corresponds to the first inverting buffer of drawing 3, The group of the second P-CH type field effect transistor 4a and the second N-CH type field effect transistor 5a corresponds to the second inverting buffer of drawing 3, The sixth P-CH type field effect transistor 4e and the sixth N-CH type field effect transistor 5e correspond to the capacitor of drawing 3, The group of the third P-CH type field effect transistor 4b, the third N-CH type field effect transistor 5b, the tenth P-CH type field effect transistor 4i, and the tenth N-CH type field effect transistor 5i corresponds to the full swing circuit of drawing 3, The group of 4 f of seventh P-CH type field effect transistor, 5f of seventh N-CH type field effect transistor, and first NOT gate 7 corresponds to the switch of drawing 2, and the remaining field effect transistors and NOT gates correspond to a full swing circuit or a switch hereafter. That is, the composition of drawing 9 combines the principle of drawing 2 and drawing 3. Because, if 4 f of seventh P-CH type field effect transistor and 5 f of seventh N-CH type field effect transistor are short-circuited, for example, It turns out well that the group of the third P-CH type field effect transistor 4b, the third N-CH type field effect transistor 5b, the tenth P-CH type field effect transistor 4i, and the tenth N-CH type field effect transistor 5i constitutes the full swing circuit. The group of 4 f of seventh P-CH type field effect transistor, 5f of seventh N-CH type field effect transistor, and first NOT gate 7, It has the same composition as drawing 7 4e, for example, the sixth P-CH type field effect transistor, the sixth N-CH type field effect transistor 5e, and the switch made in the group of first NOT gate 7. And that a switch one [a switch] and turns off in drawing 7 has only the difference which has changed to the full swing circuit to being current of an inverting buffer at drawing 9. Therefore, 4 f of seventh P-CH type field effect transistor and 5 f of seventh N-CH type field effect transistor are made one, If 4 g of eighth P-CH type field effect transistor, 5 g of eighth N-CH type field effect transistor, 4 h of ninth P-CH type field effect transistor, and 5 h of ninth N-CH type field effect transistor are turned OFF, the composition of drawing 9 will become the same as the composition of drawing 3. And since two or more full swing circuits will be connected if the field effect transistor which constitutes other switches is also made one, change of the terminal voltage of the capacitor after the terminal voltage of a capacitor in drawing 4 reaches the threshold of the second inverting buffer is accelerated more.

[0036]For example The third P-CH type field effect transistor 4b, 4 f of seventh P-CH type field effect transistor, The same current flows into the ninth P-CH type field effect transistor 4i, and The third N-CH type field effect transistor 5b, As for these sizes, since the same current flows into 5 f of seventh N-CH type field effect transistor, and the ninth N-CH type field effect transistor 5i, it is desirable to make it the same. When the field effect transistor from which a size differs is used, it is the minimum thing and current capacity is decided, and since the effect which enlarged others is lost, cautions are required.

[0037]Since the switch is not formed in the inverting buffer which becomes the last from the first P-CH type field effect transistor 4 and the first N-CH type field effect transistor 5 in drawing 9, opening and closing of a switch are free.

[0038]Drawing 10 is a sixth embodiment of the delay circuit of this invention. In drawing 10, the first P-CH type field effect transistor and 4a 4 The second P-CH type field effect transistor, The third P-CH type field effect transistor and 4c 4b The fourth P-CH type field effect transistor, The fifth P-CH type field effect transistor and 4e 4 d The sixth P-CH type field effect transistor, The seventh P-CH type field effect transistor and 4 g 4 f The eighth P-CH type field effect transistor, The ninth P-CH type field effect transistor and 4i 4 h The tenth P-CH type field effect transistor, The eleventh P-CH type field effect transistor and 4k 4j The twelfth P-CH type field effect transistor, The first N-CH type field effect transistor and 5a 5 The second N-CH type field effect transistor, The third N-CH type field effect transistor and 5c 5b The fourth N-CH type field effect transistor, The fifth N-CH type field effect transistor and 5e 5 d The sixth N-CH type field effect transistor, The ninth N-CH type field effect transistor and 5i the seventh N-CH type field effect transistor and 5 g the eighth N-CH type field effect transistor and 5 h 5 f The tenth N-CH type field effect transistor, As for the twelfth N-CH type field effect transistor and 7, 5j is [the eleventh N-CH type field effect transistor and 5k / the second NOT gate and 7b of the first NOT gate and 7a] the third NOT gate.

[0039]In the composition of drawing 10, the group of the first P-CH type field effect transistor 4 and the first N-CH type field effect transistor 5 corresponds to the first inverting buffer of drawing 3, The group of the second P-CH type field effect transistor 4a and the second N-CH type field effect transistor 5a corresponds to the second inverting buffer of drawing 3, and the sixth P-CH type field effect transistor 4e and the sixth N-CH type field effect transistor 5e correspond to the capacitor of drawing 3. If the third P-CH type field effect transistor 4b, the third N-CH type field effect transistor 5b, the tenth P-CH type field effect transistor 4i, and the tenth N-CH type field effect transistor 5i are seen as a group, it corresponds to the full swing circuit of drawing 3. The group of the third P-CH type field effect transistor 4b and the third N-CH type field effect transistor 5b Drawing 2, For example, since it corresponds to the third inverting buffer and the group of 4 f of seventh P-CH type field effect transistor, 5f of seventh N-CH type field effect transistor, and first NOT gate 7 corresponds to the switch of drawing 2, . When the third P-CH type field effect transistor 4b, the third N-CH type field effect transistor 5b, 4 f of seventh P-CH type field effect transistor, 5f of seventh N-CH type field effect transistor, and first NOT gate 7 were seen as a group, were shown in drawing 7. It corresponds to the composition which inserted the switch in the power supply [of an inverting buffer], and ground side in series. Hereafter, since the remaining field effect transistors and NOT gates also function similarly, the composition of drawing 10 combines the principle of drawing 2 and drawing 3 in a different form from drawing 9. Because, if 4 f of seventh P-CH type field effect transistor and 5 f of seventh N-CH type field effect transistor are made removal or OFF, for example, It turns out well that the group of the third P-CH type field effect transistor 4b, the third N-CH type field effect transistor 5b, the tenth P-CH type field effect transistor 4i, and the tenth N-CH type field effect transistor 5i constitutes the full swing circuit. If the tenth P-CH type field effect transistor 4i and the tenth N-CH type field effect transistor 5i are removed and seen, for example, . The third P-CH type field effect transistor 4b, the third N-CH type field effect transistor 5b, 4 f of seventh P-CH type field effect transistor, 5 f of seventh N-CH type field effect transistor, and the group of the inverting buffer 7 were shown in drawing 7. It turns out well that it has composition which inserted the switch in the power supply [of an inverting buffer], and ground side in series.

[0040]And the third P-CH type field effect transistor 4b in drawing 10, The third N-CH type field effect transistor 5b, 4 f of seventh P-CH type field effect transistor, 5 f of seventh N-CH type field effect transistor, the tenth P-CH type field effect transistor 4i, The tenth N-CH type field effect transistor 5i and the third P-CH type field effect transistor [in / in the group of a NOT gate / drawing 9] 4b, The third N-CH type field effect transistor 5b, 4 f of seventh P-CH type field effect transistor, Differing from the group of 5 f of seventh N-CH type field effect transistor, the tenth P-CH type field effect transistor 4i, the tenth N-CH type field effect transistor 5i, and a NOT gate, As opposed to 4 f of seventh P-CH type field effect transistor, the tenth P-CH type field effect transistor 4i, and 5 f of seventh N-CH type field effect transistor and the tenth N-CH type field effect transistor 5i having been connected in series in drawing 9, In drawing 10, it is the point that 4 f of seventh P-CH type field effect transistor, the tenth P-CH type field effect transistor 4i, and 5 f of seventh N-CH type field effect transistor and the tenth N-CH type field effect transistor 5i are connected in parallel. Therefore, one of the transistor from which a full swing circuit constitutes a switch, It operates regardless of OFF, and when a switch is turned on, the ON state current will flow through the third P-CH type field effect transistor 4b and the third N-CH type field effect transistor 5b which constitute an inverting buffer. for this reason, **** [the field effect transistor / the third P-CH type field effect transistor 4b that constitutes an inverting buffer in drawing 10 is designed send the current of 4 f of seventh P-CH type field effect transistor, and the tenth P-CH type field effect transistor 4i and] -- it can kick -- it does not become. This is the same also about the third N-CH type field effect transistor 5b.

[0041]In [if it designs in this way] the composition of drawing 10, While the number of the inverting buffers which send a charge and discharge current through the sixth P-CH type field effect transistor 4e and the sixth N-CH type field effect transistor 5e which are capacitors by one of each switch and control of OFF can be done in variable, Full swing operation can be made to perform.

[0042]The third P-CH type field effect transistor 4b that constitutes an inverting buffer from drawing 10, The group of the third N-CH type field effect transistor 5b, the fourth P-CH type field effect transistor 4c, Although the transistor for carrying out full swing operation altogether to the group of the group of the fourth N-CH type field effect transistor 5c, 4 d of fifth P-CH type field effect transistor, and 5 d of fifth N-CH type field effect transistor is added, This is not an indispensable thing and is good to add to one of inverting buffers.

[0043]In the above, the composition of the delay circuit of this invention was explained. In the above, although the example which constitutes a delay circuit in an inverting buffer group has been explained, the form of a buffer is not limited to this, and even if it is a non inverting buffer, it does not interfere. And when a non inverting buffer is constituted from two steps of inverting buffers, What is necessary is just to form the switch corresponding to the sixth P-CH type field effect transistor 4e of drawing 7, the sixth N-CH type field effect transistor 5e, and the first NOT gate in any the one step, What is necessary is just to establish the circuit corresponding to the second P-CH type field effect transistor 4a of drawing 3, and the second N-CH type field effect transistor 5a in any the one step, also when it constitutes a full swing circuit. What is necessary is just to insert a transmission gate in the output terminal of a non inverting buffer in series like drawing 6, in realizing a switch in a transmission gate.

[0044]Although it was above consistent and the current output type buffer explained, there is also a voltage-output type buffer. How to form a switch also about this and the method of the composition of a full swing circuit are intrinsically the same as the above-mentioned method.

[0045]Above, although it was called the "NOT gate" about one of the components of a switch, this is intrinsically the same as an inverting buffer. However, in the composition of a delay circuit, the name was only changed in consideration of the direction distinguished from the second inverting buffer becoming clear on explanation for a start [of drawing 1].

[0046]Drawing 11 is an embodiment of the digital phase locking circuit of this invention. In drawing 11, up and down and the counting circuit (a figure U/D counting circuit) 40 of a ring oscillation circuit and 20 are frequency dividers a phase comparison circuit and 30 10. A ring oscillation circuit is constituted by the delay circuit 11 and NOT gate 12.

[0047]The digital phase locking circuit of drawing 11 compares a phase with the signal which carried out dividing of the output of a ring oscillation circuit to the input clock, carries out stepping of the calculation of an up-and-down counting circuit with both phase relation, or is retreated. The binary number which is an output of this up-and-down counting circuit is supplied as one of the switch which chooses the time delay of a delay circuit, and an OFF signal. Therefore, the number of bits outputted from an up-and-down counting circuit is equal to the number of the switches of a delay circuit. If an up-and-down counting circuit shall output the enumerated data of a triplet, for example, the delay circuit of the composition of drawing 5 shall be used as the delay circuit 11 of drawing 10 like drawing 10, every 1 bit of the enumerated data of this triplet will be supplied to one terminal of the transmission gate of drawing 5. Another terminal of each transmission gate is set as common electric potential. The time delay of a delay circuit can be chosen by this.

[0048]If the time delay as which the delay circuit was chosen is made into tau_d and the time delay of NOT gate 12 is made into tau_g, the oscillating frequency of the ring oscillator 10 will be 1/. [2 (tau_d+tau_g)] -- it is -- since -- if the time delay of a delay circuit is chosen with the output of an up-and-down counting circuit as mentioned above, oscillating frequency of a ring oscillator will be changed. And the output of this ring oscillator in which the phase contrast of the signal which carried out dividing of the output of an input clock and a ring oscillator becomes the smallest serves as an output clock. This means that the stability of the output clock of a digital phase locking circuit is influenced by the accuracy of the time delay which can be chosen in a delay circuit.

[0049]Therefore, since the delay circuit of this invention can make high accuracy of the time delay which can be chosen and also the waveform distortion produced in a delay circuit can also improve it substantially as already explained in full detail, it becomes possible to also improve the stability of a digital phase locking circuit substantially.

[0050]Although omitting is also possible, it is more desirable to use a frequency divider in drawing 11, since the direction of a frequency divider which set up the oscillating frequency of the ring oscillator more highly than an input clock can improve the stability of a digital phase locking circuit.

[0051]

[Effect of the Invention]As explained in full detail above, the accuracy of the time delay which can be chosen is high and waveform distortion can also realize a small delay circuit. Thereby, it becomes possible to perform precisely phase adjustment of a clock and a data signal, and phase adjustment between data signals.

[0052]The stability of a digital phase locking circuit can be raised by using the above-mentioned delay circuit for the ring oscillator of a digital phase locking circuit.

[Translation done.]